HARDWARE

REFERENCE DESIGN

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UM220-IV NV

Automotive Grade Multi-GNSS Positioning Module

Revision History

Version	Revision History	Date
R1	UM220-IV NV-GN Hardware Reference Design (V2.0)	Aug. 2021
R1.1	Add notes about ESD protection	Nov. 2021
R1.2	Optimize the description of antenna power supply; Add Chapter 4 Power Supply Requirements	Apr. 2023

Product it applies to

This document applies to UM220-IV NV-GN, of which the PN is: 2310408000023 (V2.0).

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1 Minimum System Reference Circuit

- Supply 3.0V~3.6V power VCC
- Ground all GND pins of the module
- Connect RF_IN signal to antenna, note the 50 Ω impedance match on the circuit
- Upgrade the module via port 1, ensuring that serial port 1 can interconnect with PC through the interface
- If the user has a high requirement for ESD (> ±2000 V), the user should consider other method to feed the antenna rather than using the VCC_RF pin.

  If the antenna power supply and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on VCC, which may cause damage to the module. Therefore, it's recommended to design an independent power rail for the antenna to reduce the possibility of damage to the module.

  When designing the antenna feed circuit, it is recommended to choose a power supply chip with high ESD protection level. Gas discharge tube, varistor, TVS tube and other high-power protective devices may also be used in the power supply circuit to further protect the module from ESD damage or other Electrical Over-Stress (EOS).

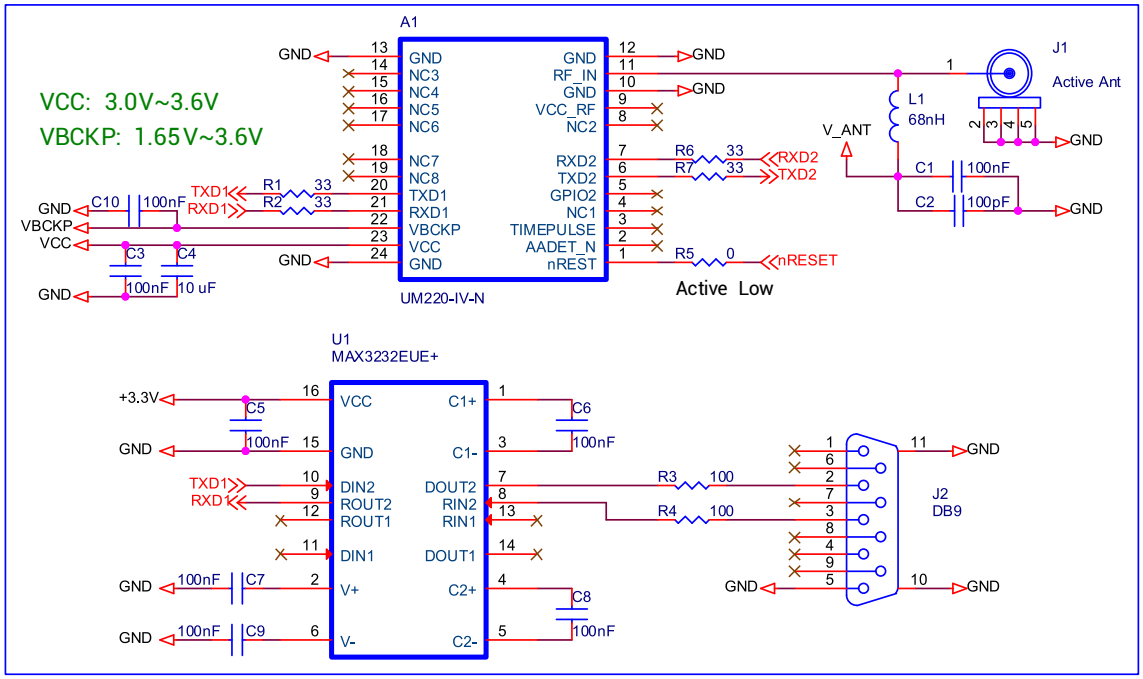

Figure 1-1 Minimum System Reference Circuit

2 Reference Circuit Using a Passive Antenna

- To ensure the system performance, low noise amplifier and filter should be added between the passive antenna and the module RF_IN
- If the user has a high requirement for ESD (> ±2000 V), the user should consider other method to power LNA rather than using VCC_RF.

  When designing circuit to power LNA, it is recommended to choose a power supply chip with high ESD protection level. Gas discharge tube, varistor, TVS tube and other high-power protective devices may also be used in the power supply circuit to further protect the module from ESD damage or other Electrical Over-Stress (EOS).
- RF wire (Antenna → LNA → SAW → RF_IN), note the impedance matching at 50Ω

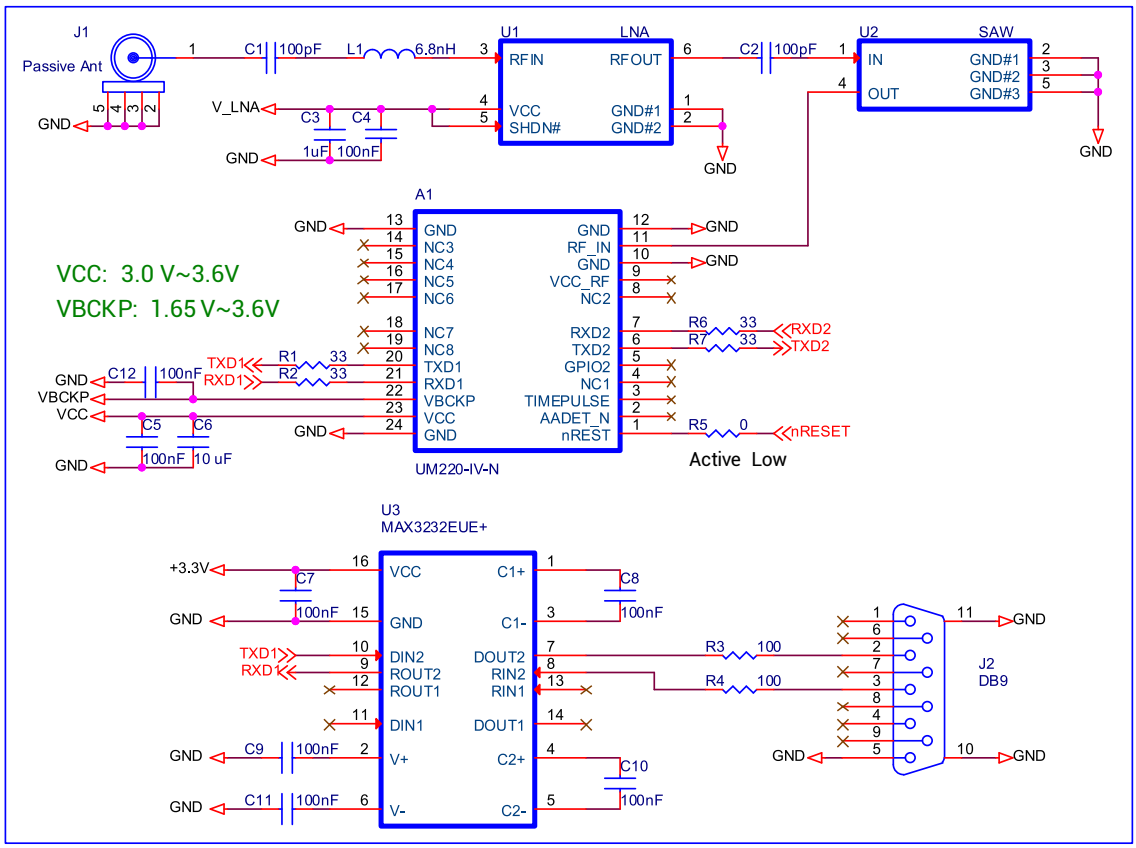

Figure 2-1 Reference Circuit Using a Passive Antenna

3 Antenna State Detection Reference Circuit

Antenna state detection uses the principle of feeding current detection, and the antenna state detection function is not supported when the antenna is not fed.

The detection circuit for the antenna state is not integrated inside the UM220-IV NV module, the antenna state detection function can be realized through the external circuit. It is suggested to add the following design to the antenna feeding circuit.

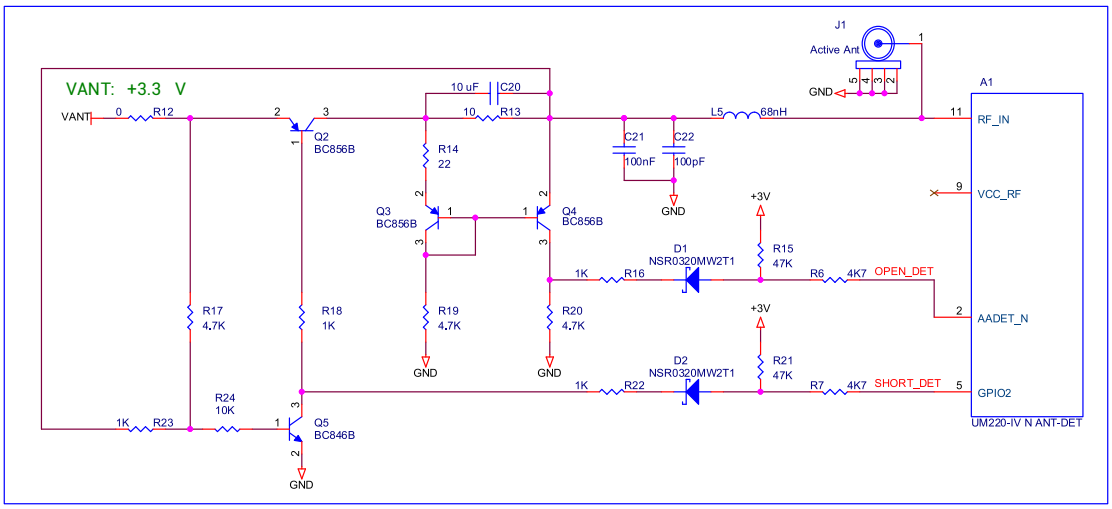

Figure 3-1 Reference Circuit of Antenna Detection

In the figure above, “VANT” is a standard +3.3 V power supply for antenna, and the antenna is fed by a 68 nH inductor at the upper right. “OPEN_DET” and “SHORT_DET” at the lower right are status indicators of the antenna, which are described in the following table, respectively.

Table 3-1 Index Signal of Antenna Detection

State	OPEN_DET	SHORT_DET
Open	HIGH	LOW
Short	LOW	HIGH
Normal	LOW	LOW

NOTE:

The antenna supply voltage in the reference circuit is +3.3 V, and the power supply current shall not exceed 80mA, if voltage and current are not in that range, adjust the parameter to ensure that SHORT_DET and OPEN_DET signals match the state values in the above table.

4 Power Supply Requirements

4.1 Main Supply (VCC)

The voltage range of VCC is 3.0 V ~ 3.6 V.

Notes:

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100 μs ~ 10 ms.
- Power-on time interval: The time interval between the power-off (VCC < 0.4 V) to the next power-on is recommended to be larger than 500 ms.

4.2 Backup Supply (V_BCKP)

If the hot start function is needed, users should supply backup power to the module. The voltage range of V_BCKP is 1.65 V ~ 3.6 V.

Notes:

- The V_BCKP initial level when power-on should be less than 0.4 V.
- The V_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V_BCKP.
- V_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 μs ~ 10 ms.
- Power-on time interval: The time interval between the power-off (V_BCKP < 0.4 V) to the next power-on is recommended to be larger than 500 ms.
- The V_BCKP pin cannot be floating or connected to ground. When V_BCKP is not used, it should be connected to VCC or connected to backup power.

5 Attachment

Avoid the leakage power

When designing the input interfaces for module UM220-IV NV, pull-up resistors are connected at the input interfaces (including RXD, GPIO as shown below) which are pulled up to VCC to prevent the impact caused by input variable state. Therefore, if there is data input on the above ports under the power-down mode, it will form leakage power on VCC, which may cause failure of startup when the module is powered on.

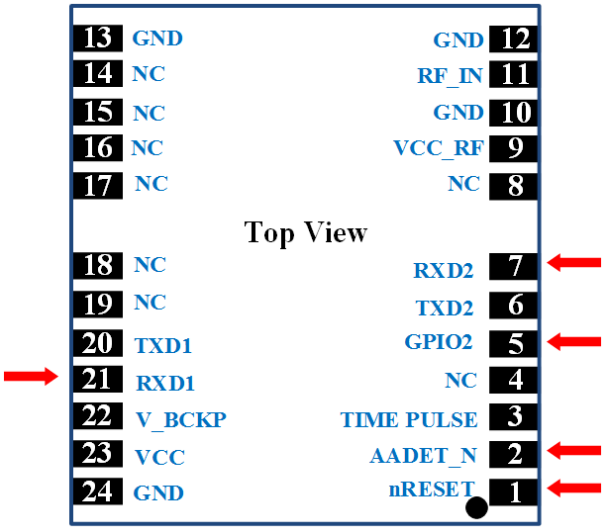

Figure 5-1 UM220-IV NV Module

Option 1

The series resistance for UART, PPS or other GPIO can avoid the abnormal operation generated when the user connects UM220-IV NV to AP or MCU applications, there is voltage through the above interface to UM220IV NV while the module powers off but AP or MCU is still at work.

- The recommended resistance value of the series resistor for PPS or other GPIO is 4.7kΩ
- The RXD and TXD pin of UART interface, as well as RESET pin, have been connected in series with the resistor inside the module, and other resistors cannot be connected in series outside the module
- No external pull-up resistor is allowed to connect with the output pin TXD

Option 2

When the module is not powered on, make sure the IO port connected to the module is in high resistance state or low level to avoid leakage power.

Note:

Because of the series resistance, the user should assess that the external equivalent pull-up resistance should be large enough (for example, greater than 10k) to avoid affecting the correct identification of the logical level. If the user is able to ensure that the external equivalent pull-up resistance of the pin is greater than 4.7k at any time, from power on to normal operation, the series resistance at the module output can be appropriately reduced.

General principle: the total pull-up resistance (including series resistance) added to the chip pin, the larger the better without affecting the logical correct identification.

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